AMENDMENTS TO THE SPECIFICATION

In the Action of June 2, 2004, the Examiner directed Applicant to amend the specification to correct an incorrect application number. Applicant appreciates the correction, and requests amendment of paragraph [0003] of the specification as shown below:

[0003] In U.S. patent application 09/560,626 filed April 28, 2000, entitled "Three-Dimensional Memory Array and Method of Fabrication," a 3D memory is described using rail-stacks which define both the lines and the memory cells of an array. Each cell includes an antifuse layer. A diode is formed once the cell is programmed. In a subsequent application, serial number 09/841~~1~~814,727 filed March 21, 2001, entitled "Three-Dimensional Memory Array and Method of Fabrication," an improved 3D memory also employing rail-stacks is described. In this application, P+N- diodes are used to reduce leakage current.